Specifications of low mass flexible cables for Layer 0 of D0 Run 2B silicon upgrade

Last revision: A.Nomerotski 2/14/02

Description of Layer 0

Tight space constrains, material budget and heat dissipation issues require the Layer 0 silicon sensors to be connected to the associated electronics with low mass flexible cables (also called in the following analog cables). Figure 1 below shows the layout of the Layer 0 sensors, analog cables and front-end readout electronics. The analog cables corresponding to different sensors will have different length.

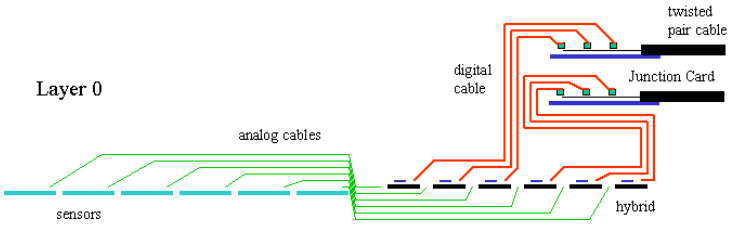

Figure 1. Layout of D0 Layer 0

At one end the cables will be wire-bonded to the silicon sensors. At the other end the cables will be wire-bonded to the hybrid as shown in Figure 2.

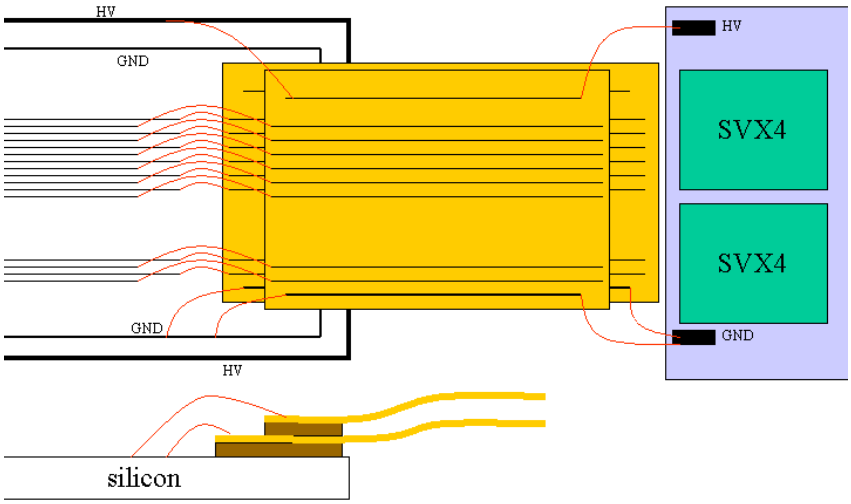

Figure 2. Analog cables are connected to a silicon sensor on the left side and to a hybrid with front-end electronics on the right side.

The pitch of signal traces on the sensors is 50 μm. The sensors have two rows of bond pads to allow for two overlapped rows of wire-bonds. Two analog cables ("top" and "bottom") with a pitch of approximately 100 μm will be glued onto a sensor. The cables will be displaced with respect to each other by half of a pitch, 50 μm, as shown in Figure 2, so the resulting assembly will have an effective pitch of 50 μm that will match the pitch of traces on the sensor. The HV and ground traces on the cable will be wire-bonded respectively to the HV and ground bias pads on the sensor and on the hybrid.

The Layer 0 will operate in harsh radiation environment and is expected to accumulate total radiation dose of 15 Mrad over period of 5 years.

Description of cables

Total of 288 analog cables will be split into 12 groups with different lengths (i.e. 24 cables have the same length – this is one group). The length of cables will vary from ~20 cm to ~45 cm. Two cables ("top" and "bottom") going to the same sensor will have length different by 2.2 mm. Figure 3 shows a schematic drawing of one cable. The cable has 129 signal traces, one HV bias trace and one ground bias trace.

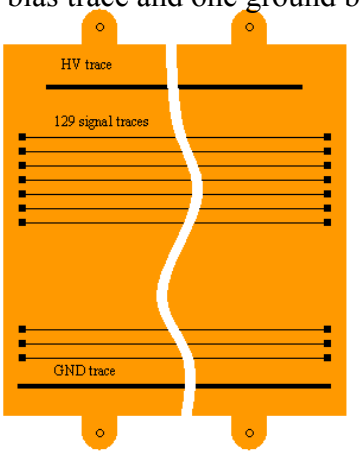

Figure 3. Schematic drawing of analog cable

The main goals for the cables are:

1. Minimal capacitance
2. Minimal material
3. Excellent continuity of the traces
4. Low cost

The substrate material is ~50 (or thinner) μm kapton and the conductor traces are ~5-10 μm gold-plated copper. The traces have the line width of 16 μm for signal lines and 100 μm for bias lines.

Specifications of cables

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1. Capacitance: < 0.40 pF/cm
2. Signal traces:
    a. Gold-plated copper
    b. Width 16±1 μm
    c. Thickness 5-8 μm
    d. Constant pitch 91±0.5 μm
    e. Bonding pads 60 μm by 150 μm
    f. 128 out of 129 traces are continuous
    g. No shorts between traces
    h. Resistance of traces < 3 Ohm/cm
    i. No protective coating on the top of the traces
3. HV and ground bias traces
    a. Gold-plated copper
    b. Width 100±5 μm
    c. Thickness 5-8 μm
    d. HV trace holds 1000 V with respect to neighboring traces
    e. HV trace is covered with coating everywhere but one mm at the ends
    f. All traces are continuous, no shorts to other traces
    g. Resistance of traces < 0.5 Ohm/cm
4. Total "bottom" prototype cable length is 420.0±0.2 mm
5. Total "top" prototype cable length is 417.8±0.2 mm
6. Length difference between "bottom" and "top" cables is 2.2±0.1 mm
7. Total prototype cable width is 13.95±0.1 mm
8. Cables has 4 ears for assembling purposes
9. Exact dimensions of the "top" and "bottom" prototype cables are specified in the attached gerber file
10. Adhesiveless copper cladding
11. Cable substrate: polyimide without halogen products (Kapton type HN or similar), thickness 50 ± 2 μm
12. All bonding pads are suitable for aluminum wedge bonding with pull strength of min 8 grams

Tests at vendor

1. Visual inspection
2. Testing for shorts and continuity
3. Selective tests of trace resistance and capacitance